Operational Amplifier Circuits

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Op-Amp & Op-Amp Circuits

Operational Amplifier (Op-Amp)

An operational amplifier is a direct coupled amplifier with two differential inputs and a single output. It is a versatile device used in almost all analog circuits. It provides very high open loop gain. It is a linear active device, which consists of different stages as show in figure.

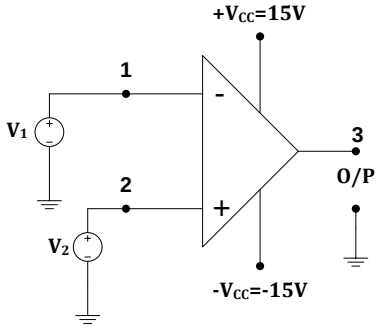


Fig: Circuit Symbol With Power Supply Connection

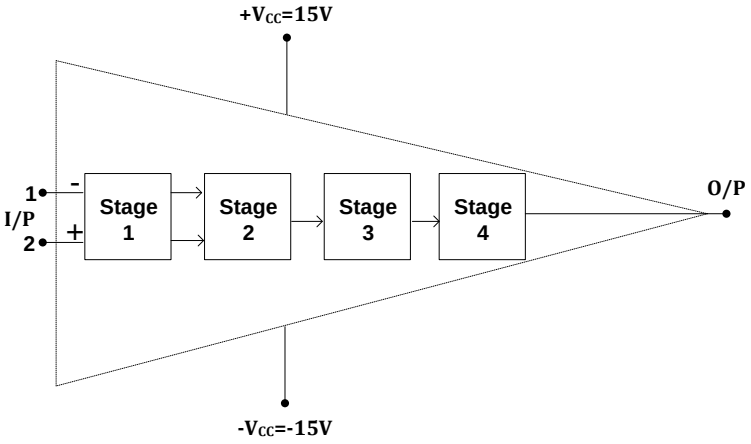


Fig: Different Stages of Operational Amplifier

Stages:

1. Differential Amplifier with Double Ended Output
2. Differential Amplifier with Single Ended Output
3. Level Shifting Amplifier
4. Emitter Follower Output Stage

It was originally designed for performing mathematical operation such as, summation, subtraction, multiplication, differentiation, integration, sigh changing etc. Now-a-days it has numerous usages e.g. scale changing analog computer operation, in instrumentation and control system and in various phase-shift and oscillator circuits.

Stage 1:
It is a differential amplifier with a non-inverting and an inverting input terminal. It has also double ended output. It has very high input impedance, so it amplifies very small signals applied differentially and rejects small and large common mode input signal.

Stage 2:
It is a medium level signal amplifier biased by constant current source. Its output is a single ended. So that it could be conveniently cascaded to the follower circuits.

Stage 3:
It is a common emitter amplifier which is responsible for level shifting as well as amplification

Stage 4:
It is basically emitter follower type circuit to obtain low output impedance and high current gain. So that it could drive the external load approximately.

Technical Characteristics: Ideal Vs. Practical Op-Amp

S.N.	Characteristics	Practical Op-Amp (NE 741)	Ideal Op-Amp
1	Voltage Gain (Open Loop)	10^5	∞
2	Input Resistance (R_{in})	$10^6\Omega$	∞
3	Output Resistance (R_{out})	75Ω	0
4	Input Bias Current	200 nA	0
5	Input Offset Current	20 nA	0
6	Input Offset Voltage	2mV	0
7	Unity Gain Band-Width	1 MHz	0 to ∞
8	Slew Rate	0.7 µV/sec	∞

Ideal Operational Amplifier

The Op-amp is designed to sense and amplify the difference between the voltages signal applied at its two input terminals. The output of Op-amp is:

$$Vo = A(V_2-V_1)$$

Where, **A** = Open loop gain.
V_2 = Voltage between terminal 2 and ground, and
V_1 = Voltage between terminal 1 and ground.

Characteristics of Ideal Operational Amplifier

1. The input impedance of an ideal Op-amp is infinity, i.e. the signal current into terminal one and two both are zero.

2. The output impedance of an ideal Op-amp is zero, i.e. the output voltage with respect to ground is always equal to $V_O = A(V_2-V_1)$ and is independent of the load.

3. It has infinite common mode rejection, i.e. it ignores any signal common to both inputs.

4. Ideal Op-amp has infinite band width, i.e. it has gain 'A' that remains constant down to zero frequency up to infinite frequency.

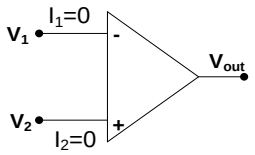


Fig: Ideal Op-Amp with Zero Signal Current Due to Infiniter I/P Impedance

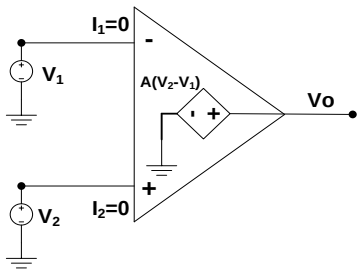


Fig: Ideal Op-Amp with Zero o/P Impedance

Virtual Short Circuit & Virtual Ground

If the Op-amp has infinite open loop gain, i.e. A→∞; and producing finite voltage at output, then voltage between the Op-amp input terminals should be negligibly constant as shown.

$$V_{out} = A(V_2 - V_1)$$

$$\text{i.e. } V_2 - V_1 = \frac{V_{out}}{A} = \frac{\infty}{A}$$

$$\text{i.e. } V_2 - V_1 = 0$$

$$\text{i.e. } V_2 = V_1$$

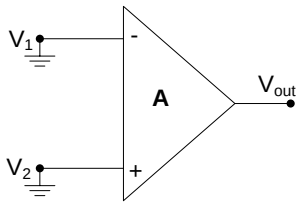


Fig: Virtual Short-Circuit & Virtual Ground

This means that, Gain (A) → ∞**;** the voltage $V_1 \rightarrow V_2$, we call this as two input terminal 'Tracking Each Other in Potential' or 'Virtual Short Circuit' exists between the two input terminals. A virtual short circuit means that whatever voltage is at terminal two, will automatically appear at terminal one because of infinite gain.

If terminal two is grounded, voltage at terminal one is zero volts, so we call the terminal one as a virtual ground.

Op-Amp Circuits

1. Inverting Configuration

In this configuration input is supplied on the inverting terminal of the op-amp, so called inverting configuration. R_2 closes loop around the op-amp, so acts as a negative feedback.

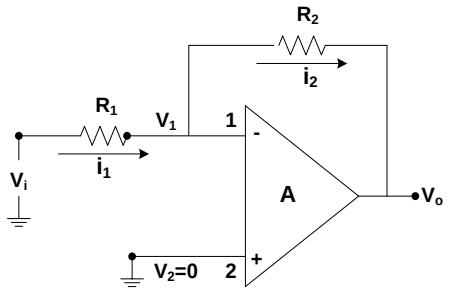


Fig: Op-Amp Inverting Configuration

Calculation of closed loop gain:

Case I: If A → Infinite (∞);

From short circuit theory: $V_2 = 0 = V_1$ and also $i_1 = i_2$ … (i)

As, $\frac{(V_i - V_1)}{R_1} = i_1$ i.e. $\frac{V_i}{R_1} = i_1$ … (ii)

Again, $V_1 = i_2 R_2 - V_o = 0$

Or, $V_o = V_1 - i_2 R_2 = -i_1 R_2 = -\frac{V_i}{R_1}.R_2$

∴ Closed loop gain $(A) = \frac{V_o}{V_i} = -\frac{R_2}{R_1}$

Case II: If A → Finite;

Then, $V_o = A(V_2 - V_1)$ i.e. $V_1 = -\frac{V_o}{A}$ … (i) ($\therefore V_2 = 0$, but $V_1 \neq V_2$)

and also, $i_1 = i_2 = \frac{(V_i - V_1)}{R_1} = \frac{V_i + \frac{V_o}{A}}{R_1}$ … ii

Again $V_o = V_1 - i_2 R_2 = V_1 - i_1 R_2 = -\frac{V_o}{A} - \frac{V_i + \frac{V_o}{A}}{R_1} R_2 = -\frac{V_o}{A} - V_i \frac{R_2}{R_1} - \frac{V_o}{A}\frac{R_2}{R_1}$

i.e. $V_o\left(1 + \frac{1}{A} + \frac{1}{A}\frac{R_2}{R_1}\right) = -V_i \frac{R_2}{R_1}$

∴Gain: $\frac{V_o}{V_i} = \frac{-\frac{R_2}{R_1}}{\left(1 + \frac{1}{A} + \frac{1}{A}\frac{R_2}{R_1}\right)} = \frac{-\frac{R_2}{R_1}}{1 + \frac{1}{A}\left(1 + \frac{R_2}{R_1}\right)}$

2. Non Inverting Configuration

Here, input is fed into the non-inverting terminal-2 of an op-amp, so called non-inverting configuration.

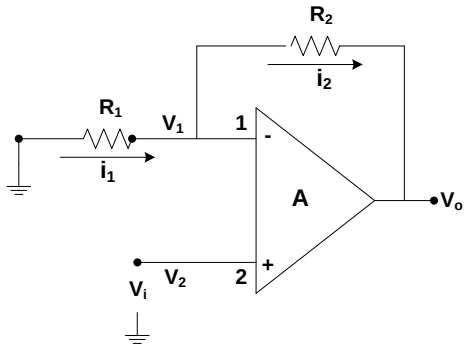


Fig: Op-Amp Non Inverting Configuration

Calculation of closed loop gain:

Case I: If A → Infinite (∞);

From short circuit theory: $V_1 = V_i$ and also, $i_1 = i_2$ … (i)

As, $\frac{(0-V_1)}{R_1} = i_1$ i.e. $i_1 = -\frac{V_i}{R_1} = i_1$ … (ii)

Again, $V_1 = i_2 R_2 - V_o = 0$

Or, $V_o = V_1 - i_2 R_2 = V_i - i_1 R_2 = V_i + \frac{V_i}{R_1}.R_2$

Or, $V_o = V_i(1 + \frac{R_2}{R_1})$

∴ Closed loop gain $(A) = \frac{V_o}{V_i} = 1 + \frac{R_2}{R_1}$

Case II: If A → Finite;

Then, $V_o = A(V_2 - V_1) = A(V_i - V_1)$ $\quad i.e. V_i - V_1 = \frac{V_o}{A}$ $\quad i.e. V_1 = V_i - \frac{V_o}{A}$ …(i)

and also, $i_1 = i_2 = \frac{(0-V_1)}{R_1} = \frac{-V_i + \frac{V_o}{A}}{R_1}$ … (ii)

Again $V_o = V_1 - i_2 R_2 = V_1 - i_1 R_2 = V_i - \frac{V_o}{A} + \frac{V_i - \frac{V_o}{A}}{R_1} R_2 = V_i - \frac{V_o}{A} - \frac{V_o}{A}\frac{R_2}{R_1} + V_i \frac{R_2}{R_1}$

i.e. $V_o(1 + \frac{1}{A} + \frac{1}{A}\frac{R_2}{R_1}) = V_i(1 + \frac{R_2}{R_1})$

∴ Gain: $\frac{V_o}{V_i} = \frac{-\frac{R_2}{R_1}}{(1+\frac{1}{A}+\frac{1}{A}\frac{R_2}{R_1})} = \frac{(1+\frac{R_2}{R_1})}{1+\frac{1}{A}(1+\frac{R_2}{R_1})}$

Design an operational amplifier having:

a) $V_o = -10V_i$ and

b) $V_o = 5V_i$

Solution:

a) When $V_o = -10V_i$

i.e. Gain (A) = $V_o/V_i = -10$

Since, it has negative voltage gain, so using a inverting configuration of op-amp, in which, $V_o = -(R_2/R_1)V_i$

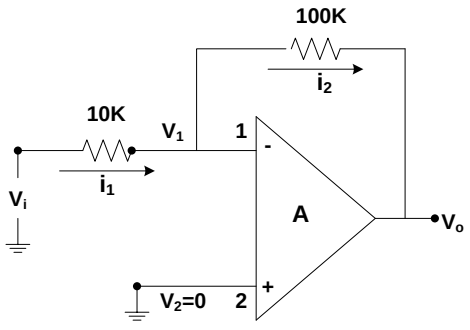
i.e. A = $V_o/V_i = -R_2/R_1$

i.e. -10 = $-R_2/R_1$

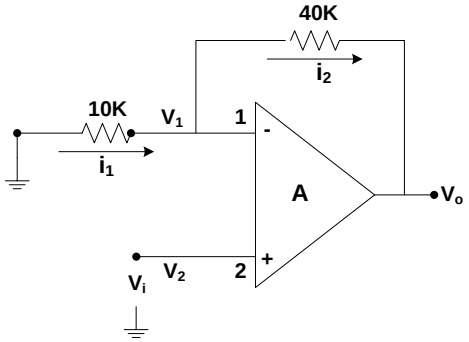
i.e. $R_2 = 10R_1$

Let; R_1 = 10K, then $R_2 = 10 \times 10 = 100K$

Now, the resulting circuit of the op-amp looks like as follow in fig(a).



Fig(a): Op-Amp Inverting Configuration



Fig(b): Op-Amp Non Inverting Configuration

b) When $V_o = 5V_i$

i.e. Gain (A) = $V_o/V_i = 5$

Since, it has positive voltage gain, so using a non-inverting configuration of op-amp, in which, $V_o = (1+R_2/R_1)V_i$

i.e. A = $V_o/V_i = 1+R_2/R_1 = (R_1+R_2)/R_1$

i.e. 5 = $(R_1+R_2)/R_1$

i.e. $5R_1 - R_1 = R_2$

i.e. $R_2 = 4R_1$

Let; R_1 = 10K, then $R_2 = 4 \times 10 = 40K$

Now, the resulting circuit of the op-amp looks like as in above fig(b).

3. The Voltage Follower

The non-inverting configuration has infinite input resistance. It enables using this circuit as a buffer amplifier to connect a source with high impedance to low impedance. Buffer amplifier has voltage gain of one.

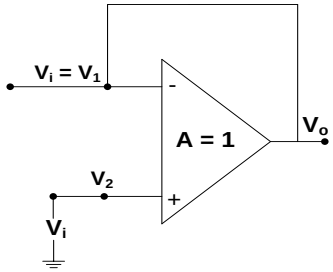


Fig: Basic Connection of Voltage Follower

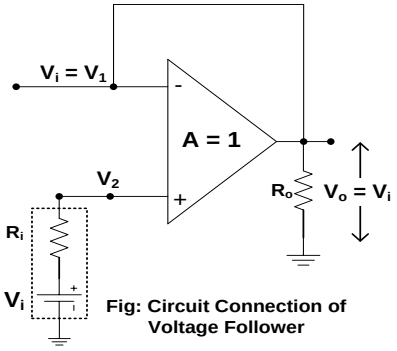


Fig: Circuit Connection of Voltage Follower

4. Integrator

It consists of a capacitor C in the feedback path of the inverting configuration.

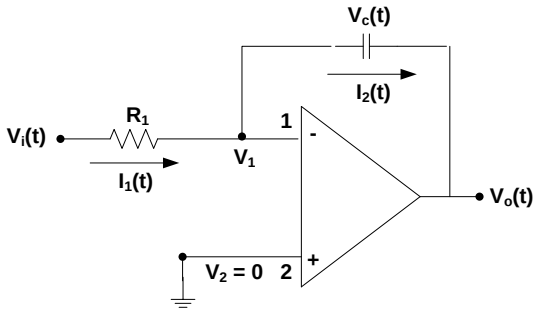


Fig: Op-amp as an Integrator

From figure:

$i_1 = \frac{\vartheta_{i(t)} - \vartheta_1}{R_1} = \frac{\vartheta_{i(t)} - 0}{R_1}$; $(\therefore V_2 = 0 = V_1)$ i.e. $i_1 = \frac{\vartheta_{i(t)} - \vartheta_1}{R_1} = \frac{\vartheta_{i(t)}}{R_1} = i_2$. …(i)

Again from loop equation:

$V_1 - \vartheta_{c(t)} - \vartheta_{o(t)} = 0$

i.e. $V_1 - \frac{1}{C}\int_0^t i_{2(t)} dt = \vartheta_{o(t)}$

i.e. $0 - \frac{1}{C}\int_0^t i_{2(t)} dt = \vartheta_{o(t)}$

i.e. $\vartheta_{o(t)} = -\frac{1}{C}\int_0^t i_{2(t)} dt$

$= -\frac{1}{C}\int_0^t \frac{\vartheta_{i(t)}}{R_1} dt$ $\{\therefore$ From … (i)$\}$

i.e. $\vartheta_{o(t)} = -\frac{1}{R_1 C}\int_0^t \vartheta_{i(t)} dt$

5. Differentiator

In this case, a capacitor C is connected in the inverting terminal -1 of the inverting configuration of an operational amplifier. In which $V_2 = 0 = V_1$.

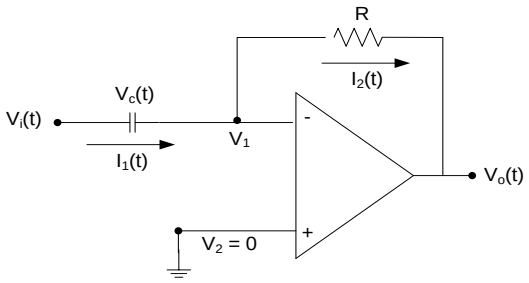


Fig: Op-amp as a Differentiator

From figure:

$\vartheta_{i(t)} - \vartheta_{c(t)} - V_1 = 0$ i.e. $\vartheta_{i(t)} = \vartheta_{c(t)}$ … (i) $(\therefore V_1 = 0)$

Since, $i_{1(t)} = C\frac{d\vartheta_{c(t)}}{dt} = C\frac{d\vartheta_{i(t)}}{dt} = i_{2(t)}$ … (ii)

Again from loop equation:

$V_1 - Ri_{2(t)} - \vartheta_{o(t)} = 0$

i.e. $\vartheta_{o(t)} = -Ri_{2(t)} = -RC\frac{d\vartheta_{i(t)}}{dt}$

i.e. $\vartheta_{o(t)} = -RC\frac{d\vartheta_{i(t)}}{dt}$

6. Difference Amplifier

Op-amp can be used in subtracting mode. The alongside figure shows a circuit that can provide the difference between two inputs.

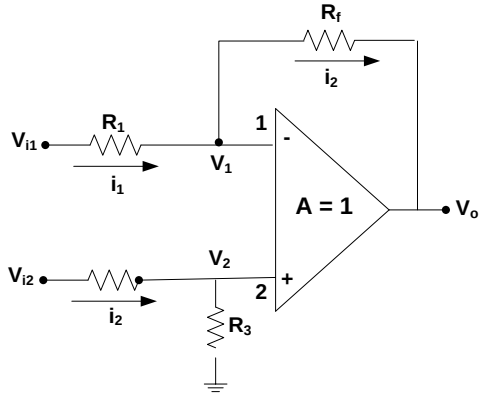


Fig: Op-amp as a Substracter

From figure, we have: $V_2 = \frac{R_3}{R_3+R_2} V_{i2} = V_1$ … (i)

As; $V_{i1} - i_1 R_1 - V_1 = 0$; i.e. $i_1 = \frac{V_{i1}-V_1}{R_1} = i_2$ … (ii)

Again from loop equation:

$V_1 - i_2 R_f - V_0 = 0$

i.e. $V_0 = V_1 - i_2 R_f = \frac{R_3}{R_3+R_2} V_{i2} - \frac{V_{i1}-V_1}{R_1} R_f$

$= \frac{R_3}{R_3+R_2} V_{i2} - \frac{V_{i1}}{R_1} R_f + \frac{V_1}{R_1} R_f$

$= \frac{R_3}{R_3+R_2} V_{i2} - \frac{R_f}{R_1} V_{i1} + \frac{R_f}{R_1} \frac{R_3}{R_3+R_2} V_{i2}$

Let: $R_f/R_1 = R_3/R_2$; then:

$V_0 = \frac{R_3/R_2}{R_3/R_2+R_2} V_{i2} - \frac{R_f}{R_1} V_{i1} + \frac{R_f}{R_1} \frac{R_3/R_2}{R_3/R_2+R_2} V_{i2}$

$= \frac{R_f/R_1}{R_f/R_1+R_2} V_{i2} - \frac{R_f}{R_1} V_{i1} + \frac{R_f}{R_1} \frac{R_f/R_1}{R_f/R_1+R_2} V_{i2}$

$= \frac{R_f}{R_1+R_f} V_{i2} - \frac{R_f}{R_1} V_{i1} + \frac{R_f}{R_1} \frac{R_f}{R_1+R_f} V_{i2}$

$= \frac{R_f}{R_1+R_f} V_{i2}(1 + \frac{R_f}{R_1}) - \frac{R_f}{R_1} V_{i1} = \frac{R_f}{R_1+R_f} V_{i2}(\frac{R_1+R_f}{R_1}) - \frac{R_f}{R_1} V_{i1} = \frac{R_f}{R_1} V_{i2} - \frac{R_f}{R_1} V_{i1}$

$\therefore \quad V_0 = \frac{R_f}{R_1}(V_{i2} - V_{i1})$

7. Comparator

Comparators are similar to Op-amp except that open loop gain is made longer by including positive feedback in the internal circuit. Due to very large open loop gain, output voltage essentially provides digital operation.

There are only two possible outputs, they are $\mathbf{V_{max}}$ and $\mathbf{V_{min}}$.

When, $\mathbf{V_{in} > V_R}$
then $\mathbf{V_o = V_{max}}$

When, $\mathbf{V_{in} < V_R}$
then $\mathbf{V_o = V_{min}}$

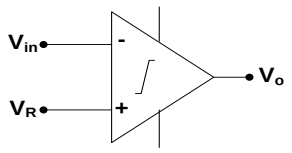


Fig: Comparator Circuit Symbol

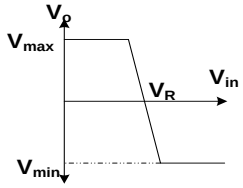


Fig: Comparator Characteristics Curve

Examples

1. **If $\vartheta_{i(t)}$ = 5sin(t), R = 100K, C = 1μF, then $\vartheta_{o(t)}$ = ?**

Solution:

We have: $\vartheta_{o(t)} = -\frac{1}{R_1 C}\int_0^t \vartheta_{i(t)}dt$

$$\vartheta_{o(t)} = -\frac{1}{100\times10^3\times1\times10^{-6}}\int_0^t 5\sin(t)dt$$

$$= -\frac{1}{100\times10^3\times1\times10^{-6}}.5\cos(t)|_0^t$$

$$= -\frac{1}{100\times10^3\times1\times10^{-6}}(5\cos t - 1)$$

$$\vartheta_{o(t)} = 50\cos t - 50$$

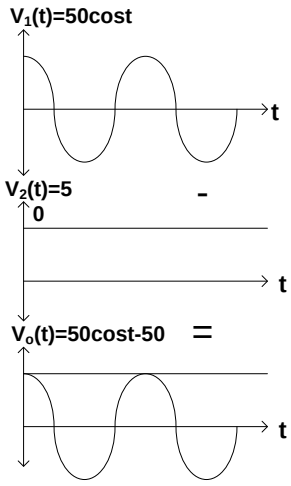


Fig: The Output of Integrator When Input is Sinusoidal

2. **If V_i = 2V, RC = 1, then V_0 = ?**

Solution:

We have: $\vartheta_{o(t)} = -\frac{1}{R_1 C}\int_0^t \vartheta_{i(t)}dt$

$$\vartheta_{o(t)} = -\frac{1}{1}\int_0^t 2dt$$

$$= -2t|_0^t$$

$$\vartheta_{o(t)} = -2t$$

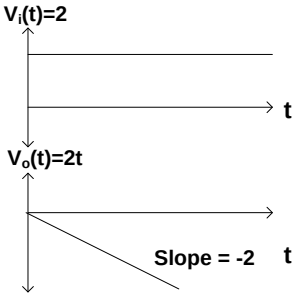


Fig: The Output of Integrator Subjected to Step Input

8. Weighted Summer

It consists of a summing of currents through the resistors at each branch supplied with corresponding input voltages. The summed current is fed to the inverting terminal of an op-amp, to which the output voltage V_0, is feed backed with resistor R_f as shown in figure alongside.

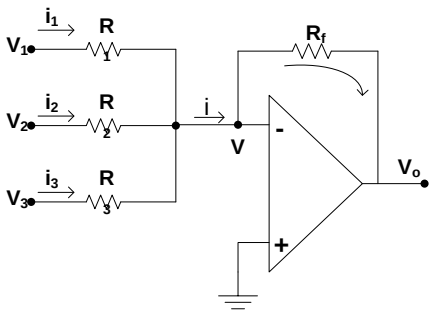


Fig: Resistor Summing Network

Here; $i_1 = \frac{V_1 - V}{R_1} = \frac{V_1 - 0}{R_1} = \frac{V_1}{R_1}$

Similarly, $i_2 = \frac{V_2}{R_2}$; $i_3 = \frac{V_3}{R_3}$ and so on.

At a junction; $i = i_1 + i_2 + i_3 + \ldots + i_n$ i.e. $i = \frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} + \cdots \frac{V_n}{R_n}$ …(i)

Again from loop equation:

$$V_1 - iR_f - V_0 = 0$$

i.e. $V_0 = -iR_f = -(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} + \cdots \frac{V_n}{R_n})R_f = \frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3 + \cdots \frac{R_f}{R_n}V_n$

Where, $\frac{R_f}{R_1}, \frac{R_f}{R_2} \ldots \frac{R_f}{R_3}$ are known as the weights of $V_1, V_2, \ldots V_n$ respectively. Since, the output voltage is the sum of all weights, so it is called by weighted summer.

Examples

1. Realize a circuit to obtain, $V_o = -2V_1+3V_2+4V_3$. Use minimum value of R as 10K.

   Solution:
   Here; $V_o = -2V_1+3V_2+4V_3 = -\{2V_1+3(-V_2)+4(-V_3)\}$ …(i)

   Comparing (i) with the equation: $V_0 = -(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3 + \cdots \frac{R_f}{R_n}V_n)$; We get:
   $\frac{R_f}{R_1} = 2$; i.e. $\frac{R_f}{2} = R_1$; $\frac{R_f}{R_2} = 3$; i.e. $\frac{R_f}{3} = R_2$ and $\frac{R_f}{R_3} = 4$; i.e. $\frac{R_f}{4} = R_3$

   Here; $R_3<R_2<R_1$; So, choosing $R_3 = 10K$. Then: $R_f = 4R_3 = 4\times10 = 40K$, $R_1 = R_f/2 = 40/2 = 20K$, $R_2 = R_f/3 = 40/3 = 13.33K$. Now, the realization of the circuit is as follow.

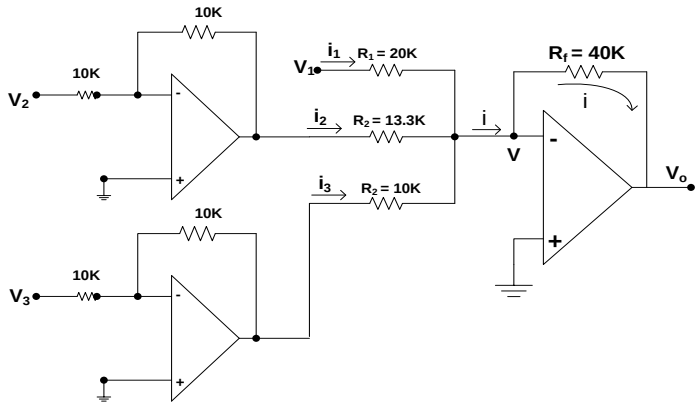


Fig: Realization of the Resistor Summing Network: When Vo = -2V₁+3V₂+4V₃

DC Imperfection of Op-Amp

Output Offset Voltage

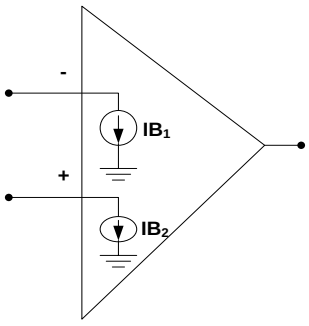
The actual value of output voltage when the inputs are zero is called the output offset voltage. It is the output level about which the signal variation occurs. If an op-amp is used only for an ac signal, it can be capacitor coupled to block the dc component represented by offset. On the other hand, at low level and low frequency signal, the offset voltage creates the error, so it has to be reduced.

Output offset voltages are the result of two distinct input phenomenons, they are;

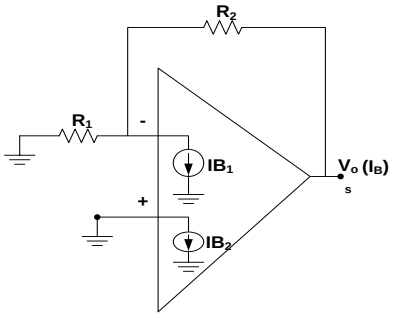
a) Input bias current and
b) Input offset voltage.

- **Input Bias Current**

  In the first-stage of op-amp i.e. differential stage, some dc bias current must flow when the transistor is properly biased. This current is called input bias current. Although, small input bias current flowing through the external resistor in an amplifier circuit produces a dc input voltage that in terms create an outpur offset voltage.



Fig(a): Input Bias Currents IB1 & IB2



Fig(b): Output Offset Voltage due to Input Bias Current

The input bias currents through two terminals are represented by two current sources I_{B1} and I_{B2} connected on two input terminals as shown below.

Generally, average input bias current is given by $I_B = (I_{B1} + I_{B2})/2$ and the difference is called input offset current, i.e. $I_{ios} = | I_{B1} - I_{B2}|$.

- **Output offset voltage for closed loop configuration due to input bias current:**

  Referring fig (b)
  $V_{os}(I_B) = R_2 \times I_{B1}$ … (i)

  So, if $R_2 \downarrow$ $V_{os} \downarrow$ Then: Gain $(-R_2/R_1) \downarrow$
  if $R_2 \uparrow$ Gain $\uparrow$ Then: $V_{os} \uparrow$
  Where V_{os} = Output offset voltage.
- **Reduction of output offset voltage due to input bias current:**

This method consists of introducing a resistance R_3 in series with the non-inverting input load as shown below.

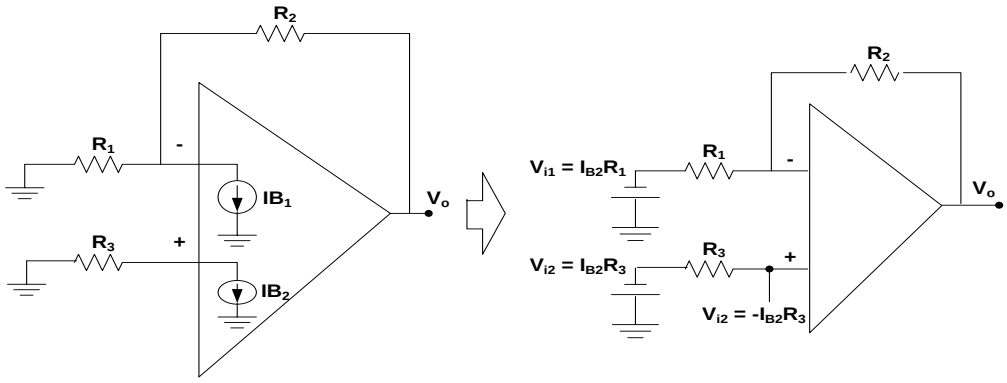


Fig: Reduction of Output Offset Voltage due to Input Bias Current by Adding Series Resistance R_3 With Non-Inverting Input Load

$\therefore$ Total output offset voltage (V_{os}) = Offset due to V_{i1} + offset due to V_{i2}

i.e. $V_{os} = V_{i1}(-R_2/R_1) + V_{i2}(1+R_2/R_1) = -I_{B1}R_1(-R_2/R_1) + (-I_{B2}R_3)(1+R_2/R_1)$

Putting $V_{os} = 0$ and assuming $I_{B1} = I_{B2} = I_B$, then:

$0 = I_BR_2 - I_BR_3(1+R_2/R_1)$

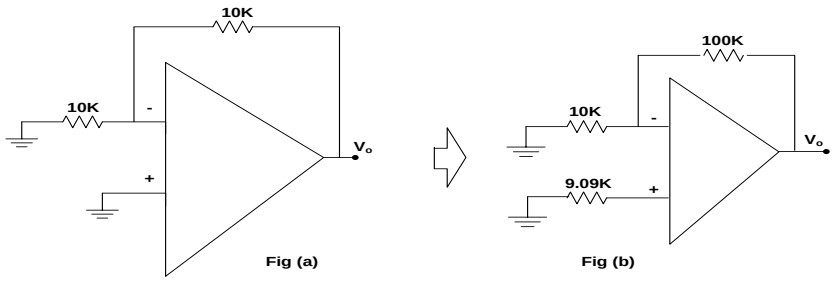
i.e. $R_3 = R_2/(1+R_2/R_1) = R_1R_2/(R_1+R_2) = R_1 // R_2$

$\therefore$ $R_3 = R_1 // R_2$

Where R_3 is called a compensation resistor.

Examples

1. Calculate the output offset voltage due to 300nA of bias current. How can you reduce this offset voltage?



Solution:

Given; I_B = 300 nA, i.e. $I_{B1} = I_B$ = 300 nA; R_1 = 10K and R_2 = 100K

a) $V_{OS}(I_B) = R_2.I_{B1} = 10010^3 \times 300 \times 10^{-9} = 0.3$ mV

b) In order to reduce this offset voltage, an external resistance R_3 should be connected in series at terminal-2, for which $R_3 = R_1//R_2 = 10K//100K = 9.09K$

Now, the resulting circuit will be as give in above fig (b).

Note: We have, $R_3 = R_1//R_2$ (only for $I_B = I_{B1} = I_{B2}$). If $I_{B1} \neq I_{B2}$; it should be noted that inserting R_3 in terminal-2 cannot nullify the offset voltage but in this case output offset voltage is given by: $V_{OS} = I_{OS}.R_2 = |I_{B1} - I_{B2}|.R_2$

2. Given $I_B = 80nA$, IOS = 10nA, $R_1 = 10K$ and $R_2 = 100K$ (Note: $I_{B2} > I_{B1}$)
   Find:
   a) Optimum value of compensation resistor.
   b) Offset voltage with compensation resistor.
   c) Offset voltage without compensation resistor.

Solution:

Since, $I_B = (I_{B1} + I_{B2})/2 = I_{B1} + I_{B2} = 80\times2 = 160$ … (i)
And $I_{OS} = |I_{B1} - I_{B2}| = |I_{B2} - I_{B1}| = 10$ … (ii)
Solving I and II, we get: $I_{B1} = 75nA$ and $I_{B2} = 85nA$

Now,
a) $R_3 = R_1//R_2 = 10K//100K = 9.09K$
b) $V_{OS} = I_{OS}.R_2 = 10\times10^{-9}\times100\times10^3 = 1mV$
c) V_{OS}(without R_3) $= I_{B1}.R_2 = 75\times10^{-9}\times100\times10^3 = 7.5mV$.

- **Input Offset Voltage**

Another input phenomenon that contributes to output offset voltage as an internally generated potential difference that exists because of imperfect matching of the input transistors. This internally generated potential difference is called input offset voltage. In another words, input offset voltage can be defined as the voltage required to supply through the input to make the output offset voltage zero.

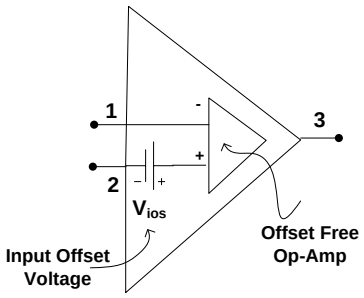


Fig: Demonstration of Input Offset Voltage

The effect of this voltage can be analyzed by modeling op-amp as shown in above figure. It consists of a dc source of value V_{ios} placed in series with the input load of an offset free op-amp.

- **Output offset voltage of a closed loop op-amp configuration due to input offset voltage.**

Here;
$i_1 = i_2$ and $V_1 = V_{ios}$

$i_1 = -V_1/R_1 = -V_{ios}/R_1$

Again;

$V_{os} = V_1 - i_2R_2$
$= V_{ios} - i_1R_2$
$= V_{ios} + V_{ios}.(R_2/R_1)$
$\therefore V_{os} = V_{ios}\{1+(R_2/R_1)\}$

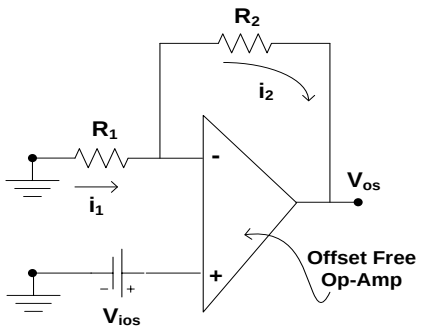


Fig: Demonstration of Output Offset Voltage of Closed Loop Op-Amp Configuration Due to Input Offset Voltage

Hence; total offset voltage is given by:
V_{tos} = Offset voltage due to i/p bias current + Offset voltage due to i/p offset voltage
i.e. $V_{tos} = I_{B1}.R_2 + V_{ios}\{1+(R_2/R_1)\}$

This is the case when compensation resistor is not used. When compensation resistor R_3 is used, then: $V_{tos} = I_{OS}.R_2 + V_{ios}\{1+(R_2/R_1)\}$; Where, $R_3 = R_1/R_2$

Examples:

1. Given: $R_1 = 15K$, $R_2 = 75K$, $I_B = 100nA$, $I_{Os} = 20nA$, $V_{ios} = 0.5mV$. Find V_{tos} when;
   a) Compensation resistor is used under the assumption of i) $I_{B1}>I_{B2}$, ii) $I_{B2}>I_{B1}$.
   b) Compensating resistor is not used as i) $I_{B1}>I_{B2}$, ii) $I_{B2}>I_{B1}$.
   c) Find R_3 ie; compensating resistor.

Solution:

a) When R_3 is used:

$V_{os1} = I_{os}.R_2 = 20\times10^{-9}\times75\times10^3 = 1.5$ mV
$V_{os2} = I_{os}.\{1+(R_2/R_1)\} = 0.5(1+75/15) = 3$ mV
$V_{tos} = V_{os1} + V_{os2} = 3 + 1.5 = 4.5$ mV (for both case i and ii)

b) When R_3 is not used:

i) If $I_{B1}>I_{B2}$
Then, $I_{os} = |I_{B1} - I_{B2}| = 20$ nA
i.e. $I_{B1} - I_{B2} = 20nA$ …(i) and $I_B = (I_{B1}+I_{B2})/2$, i.e. $I_{B1}+I_{B2} = 200nA$ … (ii)
Solving i and ii, we get: $I_{B1} = 110nA$ and $I_{B2} = 90nA$

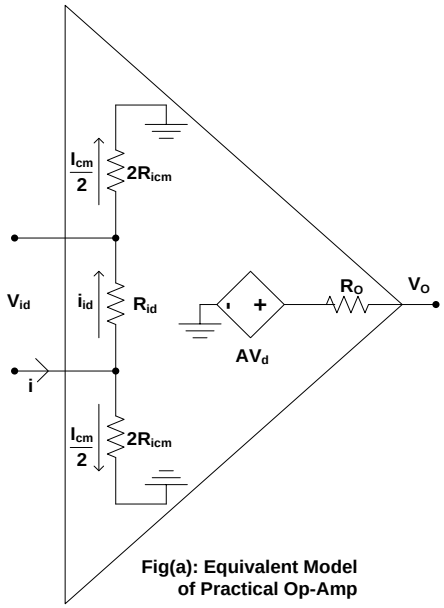
Now; $V_{tos} = V_{os1} + V_{os2}$
$= I_{B1}.R_2 + 3mV$
$= 110\times10^{-9}\times75\times10^3 + 3mV = 11.25$ mV

ii) If $I_{B1} < I_{B2}$
Then, from similar calculation we get: $I_{B1} = 90nA$ and $I_{B2} = 110nA$

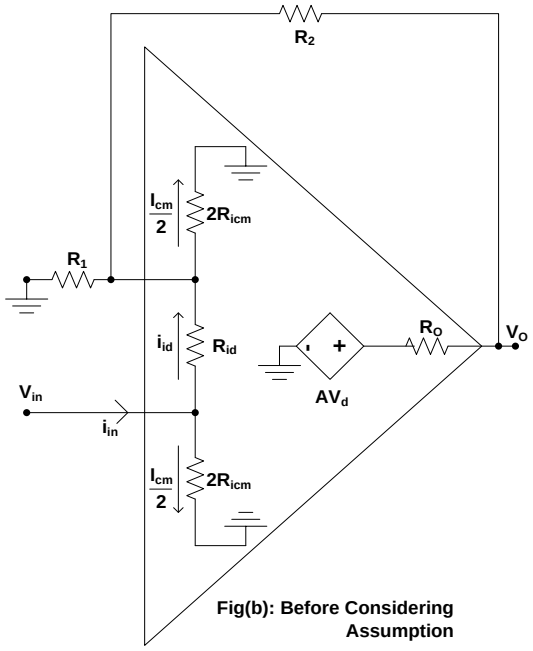
$\therefore V_{tos} = V_{os1} + V_{os2}$
$= I_{B1}.R_2 + 3mV$
$= 90\times10^{-9}\times75\times10^{3} + 3mV = 9.75\ mV$

c) Compensation resistor, $R_3 = R_1 // R_2 = 75K // 15K = 12.5K$

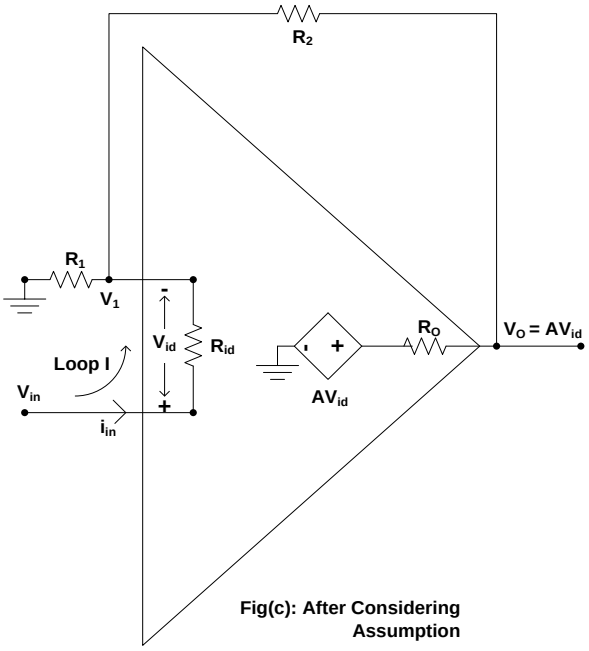
Equivalent Model of Practical Op-Amp



Fig(a): Equivalent Model of Practical Op-Amp



Fig(b): Before Considering Assumption



Fig(c): After Considering Assumption

Legends:

R_{icm} = Common mode resistance between terminal and ground
i_{cm} = Common mode current
R_{id} = Differential resistance between two terminal.
i_{id} = Differential current.
A = Open loop gain of op-amp
R_o = Output resistance of Op-amp

For input resistance of non-inverting configuration: $R_1 << R_{icm}$
i.e. $R_o \approx 0$ and $2R_{icm} >> R_{id}$

Therefore, input impedance of non inverting configuration is very high while that of inverting configuration is very low.

Referring fig: c) $V_1 = \frac{R_1}{R_1+R_2} \times V_O$

If $\frac{R_1}{R_1+R_2} =$; then: $V_1 = \beta V_o$ …(i)

From loop I
$V_{in} - i_{in}R_{id} - V_1 = 0$ i.e. $V_{in} = V_{id} + V_1$

Now;
R_{in} = Input terminal resistance = input voltage/input current

i.e. $R_{in} = V_{in}/i_{in}$

i.e. $R_{in} = \frac{V_{id}+V_1}{i_{id}} = \frac{V_{id}+V_1}{V_{id}/R_{id}} = \frac{V_{id}+\beta V_o}{V_{id}/R_{id}} = \frac{V_{id}+\beta A V_{id}}{V_{id}/R_{id}} = \frac{(1+A\beta)V_{id}}{V_{id}R_{id}} = \frac{(1+A\beta)}{R_{id}}$

i.e. $R_{in} = \frac{(1+A\beta)}{R_{id}}$

Output Impedance of Closed Loop Op-Amp

To find output resistance, input sources are made short and grounded. Applying a test voltage at output resistance, $R_{out} = V_x/I_x$.

Let us assume, $R_{icm} \to \infty$ and $R_{id} >> R_1$ i.e. $R_{id}//R_1 = R_1$

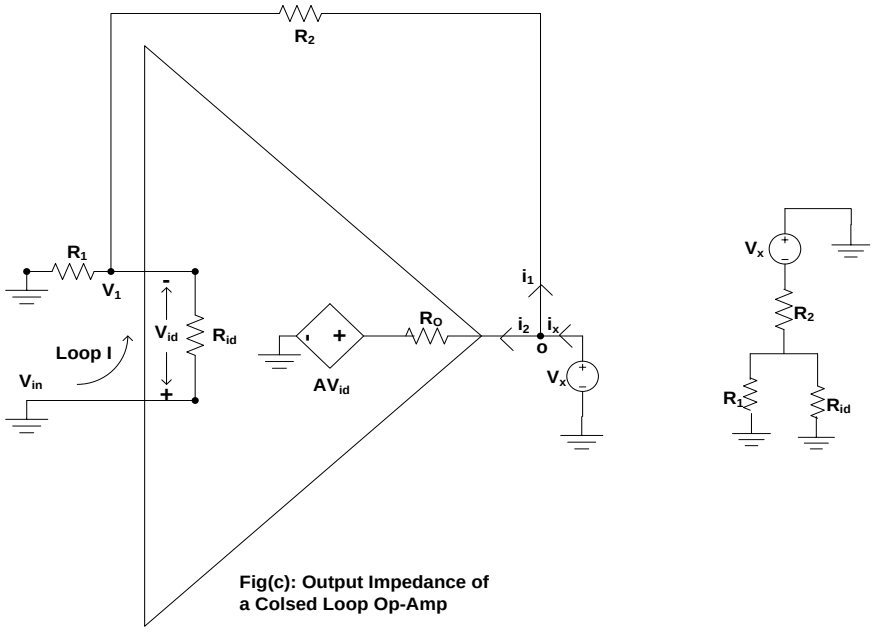
Now;
$V_1 = \frac{R_2}{R_1+R_2} \times V_x = \beta V_x$ i.e. $V_1 = \beta V_x$ …(i)

At junction 'O' $i_x = i_1 + i_2$ …(ii)

But:

$i_1 = \frac{V_x}{R_1//R_{id}+R_2} = \frac{V_x}{R_1+R_2}$ and

$i_2 = \frac{V_x - AV_d}{R_o} = \frac{V_x - A(0-V_1)}{R_o} = \frac{V_x + AV_1}{R_o} = \frac{V_x + A\beta V_x}{R_o} = \frac{V_x}{R_o}(1 + A\beta)$



Fig(c): Output Impedance of a Colsed Loop Op-Amp

$\therefore \quad i_x = i_1 + i_2$

i.e. $i_x = \frac{V_x}{R_1+R_2} + \frac{V_x}{R_o}(1 + A\beta) = V_x\{\frac{1}{R_1+R_2} + \frac{(1+A\beta)}{R_o}\}$

i.e. $\frac{i_x}{V_x} = \frac{1}{R_1+R_2} + \frac{(1+A\beta)}{R_o}$

i.e. $\frac{1}{R_{out}} = \frac{1}{R_1+R_2} + \frac{1}{R_o/(1+A\beta)}$

i.e. $R_{out} = (R_1 + R_2)//\{R_o/(1 + A\beta)\}$

If gain is high then: $R_o/(1+AB)$ becomes low.

i.e. $\frac{1}{R_o/(1+A\beta)} \gg (R_1 + R_2)$

So, for parallel case; $R_{out} = R_o/(1 + A\beta)$

Common Mode Rejection Ratio (CMRR)

The operational amplifier basically operates to amplify the difference between the signals applied across its two terminals i.e. it is intended to operate in differential mode. So, when input terminals are tied together, the output voltage should be ideally zero but due to some imperfections within an actual op-amp, some common mode voltage will appear at the output. The ratio of output common mode voltage to input common mode voltage is called common mode voltage gain.

$$\text{i.e. } A_{CM} = \frac{V_{ocm}}{V_{icm}}$$

Now;
CMRR is defined as the ration of differential gain A_d to common mode gain A_{cm}.

$$\text{i.e. } CMRR = \frac{A_d}{A_{cm}}$$

Since, $A_d >> A_{cm}$, CMRR is very high, so it is expressed in dB.

$$\text{i.e. } CMRR = 20\log\left(\frac{A_d}{A_{cm}}\right)\text{dB}$$

Typically CMRR ranges from 80dB to 100dB. The op-amps with high CMRR will be least affected by noise signals, that are common to both terminals because of higher ability to reject the common mode signals.

- **Output voltage in terms of CMRR**

  Since, Output voltage = Output voltage due to differential mode + Output voltage due to common mode

  $$\text{i.e. } V_o = A_d V_d\left(1 + \frac{A_{cm}}{A_d}.\frac{V_{icm}}{V_d}\right) = A_d V_d\left(1 + \frac{1}{CMRR}.\frac{V_{icm}}{V_d}\right)$$

  Where;

  A_d = Differential Gain
  V_d = Differential Voltage
  A_{cm} = Common mode gain
  V_{icm} = Common mode input voltage

Example

The input terminals of an op-amp are connected to voltage signals of strength 745 µV and 740 µV respectively. The gain of the op-amp in differential mode is 5×10^5 and its CMRR is 80 dB. Calculate the output voltage and percentage error due to common mode.

Solution

$V_d = |V_2 - V_1| = |740\text{-}745| = 5\times10^{-6}$ V

$A_d = 5\times10^5$ and CMRR = 80dB

As: . $V_o = A_d V_d(1 + \frac{1}{CMRR}.\frac{V_{icm}}{V_d}) = 5\times10^5 \times 5\times10^{-6}(1 + \frac{1}{CMRR}.\frac{V_{icm}}{5\times10^{-6}})$

Where, $V_{icm} = V_{cm} = (740+745)/2 = 742.5$ μV and

$(CMRR)_{dB}$ = 20log(CMRR)
i.e. 80 = 20log(CMRR)
i.e. CMRR = 10^4

$\therefore V_o = 5\times10^5 \times 5\times10^{-6}(1 + \frac{1}{10^4}.\frac{742.5\times10^{-6}}{5\times10^{-6}}) = 2.537V$

%-age error = $\frac{\text{Output Voltage due to common mode}}{\text{Total Output Voltage}} \times 100$

$= \frac{V_{cm}\times A_{cm}}{2.537} \times 100$

$= \frac{V_{cm}\times\frac{A_d}{CMRR}}{2.537} \times 100$

$= \frac{742.5\times\frac{5\times10^5}{10^4}}{2.537} \times 100 = 1.46\%$

Power Supply Rejection Ratio (PSRR)

PSRR is defined as the ration of change in output voltage to change in power supply.

i.e. PSRR = $\frac{\Delta V_O}{\Delta V_S}$

PSRR is considered as the measure of ability of op-amp to ignore changes in power supply.